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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/587,691
Filing Date: July 27, 2006
Appellant(s): HOFMANN, HANNES P.

Thomas W. Adams
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/02/2011 appealing from the Office action mailed 10/12/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims pending: 1-24

Claims rejected: 1-24

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(**5) Summary of Claimed Subject Matter**

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any

advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

2002/0177006	Clothier et al.	11-2002
6,240,636	Asai et al.	6-2001
5,666,722	Tamm et al.	9-1997
2002/0129972	Konrad et al.	9-2002
4,740,416	Yokogawa et al.	5-2004
5,577,309	Frank et al.	11-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 10, 12-14, 21 and 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Clothier et al. (US Pub. 2002/0177006) in view of Asai et al. (US Pat. 6,240,636) (previously cited).

Regarding claim 1, Clothier et al. discloses a structure having flush circuitry features and method of making comprising: providing a carrier foil (1, Fig. 2a) ; coating the carrier foil (1, Fig. 2A) on at least one side thereof with a dielectric (3, Fig. 2C) to form a dielectric layer; structuring the dielectric layer for producing trenches 4 (Fig. 2C) therein using laser ablation (Par. 42), the trenches not extending completely through the dielectric layer to the circuit traces and the vias extending through the dielectric layer to the circuit traces (Fig. 2C shown the trenches not extending completely through the dielectric layer 3); depositing a primer onto the entire surface of the dielectric layer or depositing the primer layer into the produced trenches (Par. 45); depositing a metal layer (5, Fig. 2D) onto the primer layer, with the trenches being completely filled with metal for forming conductor structures therein; removing the metal layer (Fig. 2E) and the primer layer, except for in the trenches and vias, to expose the dielectric layer if the primer layer has been deposited onto the entire surface in method step. Clothier does not disclose providing a printed circuit board having a circuit traces on at least one side thereof; structuring the dielectric layer for producing vias; and the vias extending through the dielectric layer to the circuit traces. Asai et al. discloses providing a printed circuit board (Fig. 1) having a circuit traces (3, Fig. 1) on at least one side thereof and structuring the dielectric layer for producing vias (5, Fig.1) using laser ablation; and the vias (5, Fig. 1) extending through the

dielectric layer to the circuit traces. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in Clothier et al., providing a printed circuit board having a circuit traces on at least one side thereof; structuring the dielectric layer for producing vias; and the vias extending through the dielectric layer to the circuit traces, as taught by Asai et al., in order to fabricate multilayer interconnect printed circuit board.

Regarding claim 10, Clothier further discloses further method steps are performed one or several times after method step (f); depositing another dielectric layer onto the dielectric layer being provided with trenched and vias; and repeating the step © through (f) (Par. 51)

Regarding claim 12, Clothier et al. further discloses the primer layer is deposited by sputtering or by a direct deposition method (Par. 45-46).

Regarding claim 13, Clothier et al. further discloses a method of manufacturing printed circuit board wherein the metal layer is formed by electroless plating (Par. 45-46).

Regarding claim 14, Clothier et al. further discloses a method of manufacturing printed circuit board wherein the metal layer and the primer layer are removed by polishing (Par. 47).

Regarding claim 21, Clothier et al. further discloses a method of manufacturing printed circuit board wherein a method of manufacturing printed circuit board where the printed circuit board is a multilayer circuit board comprising two sides and a conductor pattern on each side (Fig. 2).

Regarding claim 24, Asai et al. further discloses the laser ablation comprises contacting the dielectric layer with reactive gas during the laser ablation (Fig. 1).

Claims 2-11, 15 and 18-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Clothier et al. (US Pub. 2002/0177006) in view of Asai et al. (US Pat. 6,240,636) and further view Tamm et al. (US Pat. 5,666,722) (Previously cited).

Regarding claim 2, Clothier/Asai disclose substantially all features of the claimed invention as set forth above **except** the trenches and vias are produced in one single process operation in method step. Tamm discloses trenches (24, 25 and 26 Fig. 2b) and vias (23a, Fig. 2c) are produced in one single process operation in method step (Col. 4, Lines 50-54; Col. 4, Line 66 to Col. 5, Line 2). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in Clothier/Asai, the trenches and vias are produced in one single process operation in method step, as taught by Tamm et al., in order to simplify the process of manufacturing the printed circuit board.

Regarding claim 3 and 20, Tamm further discloses a method of manufacturing printed circuit board where the trenches and vias are performed by a laser ablation with direct-writing technique (Col. 6, Lines 17-24).

Regarding claim 4, Tamm further discloses a method of manufacturing printed circuit board where the direct-write technique comprises scanning a laser beam across the dielectric layer at those surface regions of the dielectric in which the trenches and vias are to be produced (Col. 6, Lines 17-45).

Regarding claims 5 and 18, Tamm further discloses a method of manufacturing printed circuit board which adjusting the power of the laser beam to depend on the depth of the trenches and vias to be produced (Col. 3, Lines 38-40; Col. 6, Lines 45-47).

Regarding claim 6, Tamm further discloses a method of manufacturing printed circuit board where the direct-write technique further comprises pulsing the laser beam (Col. 3, Lines 29-33).

Regarding claim 7, Tamm further discloses a method of manufacturing printed circuit board where adjusting the energy amount of the laser beam irradiated to a surface area of the dielectric layer to depend on the depth of the trenches and vias to be produced by setting the number of laser pulses being irradiated to said surface area (Col. 3, Line 38-43).

Regarding claims 8 and 22, Tamm further discloses a method of manufacturing printed circuit board where the direct-write technique further comprises decreasing the energy amount of successive energy pulses being irradiated to a surface area of the dielectric layer (Col. 3, Line 38-43).

Regarding claim 9, Tamm further discloses a method of manufacturing printed circuit board where the trenches are connected to another trenches in different layers for multilayer board (Fig. 2f).

Regarding claim 10, Tamm further discloses a method wherein further method steps are performed once or several times after method step f): g) Depositing another dielectric layer onto the dielectric layer being provided with

trenches and vias; and h) Repeating the steps c through f (Fig. 1g; Col. 4, Lines 42-49).

Regarding claims 11 and 19, Tamm further discloses a method of manufacturing printed circuit board wherein a terminating layer 12 and 13 (Fig. 1g) is deposited after any one of method steps f or h (Col. 4, Lines 42-49).

Regarding claim 15, Tamm further discloses a method of manufacturing printed circuit board wherein producing trenches and vias in the dielectric in method step c comprises producing trenches, said trenches also comprising vias (Fig. 2b-2c).

Regarding claim 21, Tamm further discloses a method of manufacturing printed circuit board wherein a method of manufacturing printed circuit board where the printed circuit board is a multilayer circuit board comprising two sides and a conductor pattern on each side (Fig. 2f) (Col. 4, Lines 32-35).

Claim 16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Clothier et al. (US Pub. 2002/0177006) in view of Asai et al. (US Pat. 6,240,636) and further view of Konrad et al. (US Pub. 2002/0129972) (Previously cited).

Regarding claim 16, Clothier/Asai disclose substantially all features of the claimed invention as set forth above **except** the functional layers are deposited onto the metal layer for electrically contacting electric components. Konrad et al. discloses the functional layers are deposited onto the metal layer for electrically contacting electric components (Par. 49). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in

Clothier/Asai, the functional layers are deposited onto the metal layer for electrically contacting electric components, as taught by Konrad et al., in order to have a excellent conductive layer that makes contact with semiconductor chip.

Claim 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Clothier et al. (US Pub. 2002/0177006) in view of Asai et al. (US Pat. 6,240,636) and further view of Yokogawa et al. (US Pat. 6,740,416) (Previously cited).

Regarding claim 17, Clothier/Asai disclose all the claimed features as set forth above **except** the circuit carrier is manufactured in a horizontal line. Yokogawa et al. discloses the circuit carrier is manufactured in a horizontal line (Col. 18, Line 53 to Col. 19, Lines 8). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in Clothier/Asai, the circuit carrier is manufactured in a horizontal line, as taught by Yokogawa et al., in order to simplify the process of manufacture the printed circuit board.

Claim 23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Clothier et al. (US Pub. 2002/0177006) in view of Asai et al. (US Pat. 6,240,636) and further view of Frank et al. (US Pat. 5,577,309) (previously cited).

Regarding claim 23, Clothier/Asai disclose all the claimed features as set forth above including from Asai, the vias (5, Fig. 1) have a V shape cross section **except** the trenches have a V-shape cross section. Frank et al. discloses the trenches 22 (Fig. 1) and (23, Fig. 1) have a V-shape cross section. It would

have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in Clothier/Asai, the trenches have a V-shape cross section, in order to simply the laser etching step.

(10) Response to Argument

B. Rejection of Claims 1, 10, 12-14, 21 and 24 as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636) should be reversed.

2. The Rejections Based on Clothier Are Clearly Erroneous

Appellant argues "Thus, the teachings of these references are not compatible with one another, and would not have rendered obvious the invention. Thus, in order to combine these references, such a fundamental change would be necessary in clothier that it would completely alter the basic function of the teachings of the reference, and such extreme modification, to the point of destroying the function of the inventions disclosed in the references, is not proper for any obviousness analysis. Such a major modification would not have been obvious to a person of ordinary skill in the art, and thus the contended result of this modification would not have been obvious, either. Therefore, for this reason, the two references, Clothier and Asai, do not suggest the combination of the method as claimed. Since all the rejections are based on this clearly erroneous combination, none of the rejections state a proper prima facie case of obviousness and should be reversed". The Examiner respectfully disagrees. As discussed in the Final office action, Clothier et al. discloses a structure having

flush circuitry features and method of making comprising: providing a carrier foil (1, Fig. 2a) ; coating the carrier foil (1, Fig. 2A) on at least one side thereof with a dielectric (3, Fig. 2C) to form a dielectric layer; structuring the dielectric layer for producing trenches 4 (Fig. 2C) therein using laser ablation (Par. 42), the trenches not extending completely through the dielectric layer to the circuit traces and the vias extending through the dielectric layer to the circuit traces (Fig. 2C shown the trenches not extending completely through the dielectric layer 3); depositing a primer onto the entire surface of the dielectric layer or depositing the primer layer into the produced trenches (Par. 45); depositing a metal layer (5, Fig. 2D) onto the primer layer, with the trenches being completely filled with metal for forming conductor structures therein; removing the metal layer (Fig. 2E) and the primer layer, except for in the trenches and vias, to expose the dielectric layer if the primer layer has been deposited onto the entire surface in method step. Clothier et al. does not disclose providing a printed circuit board having circuit traces on at least one side thereof; structuring the dielectric layer for producing vias; and the vias extending through the dielectric layer to the circuit traces. However, Asai discloses providing a PCB circuit board (Fig. 1 shown a PCB having circuit traces 3 on at least one side thereof); structuring the dielectric layer for producing vias (5, Fig. 1) using laser ablation; and the vias (5, Fig. 1) extending through the dielectric layer to the circuit traces (3). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize in Clothier et al., providing a printed circuit board having a circuit traces on at least one side thereof; structuring the dielectric layer for producing vias; and the vias extending

through the dielectric layer to the circuit traces, as taught by Asai et al., in order to fabricate multilayer interconnect printed circuit board. Clothier et al. and Asai et al. are related to manufacturing a printed circuit board therefore, one ordinary skill in the art would combine these references. According to the MPEP chapter 2111.03 [R-3], the transitional phrase "comprising" is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. Therefore, the claims do not exclude the additional steps disclose by Clothier et al.
The rejection relies on a PCB having circuit traces as taught by Asai et al. and performs the method as disclosed by Clothier et al. to produce the product as claimed by the Appellant.

3. The Examiner Failed to Rebut Appellant's Facts and Arguments.

Appellant argues "the Examiner's interpretation of the 'can be' in [0049] is clearly incorrect and is not in accordance with the English language. Appellant respectfully submits that this is interpretation is clearly erroneous and with out support of any evidence, much less substantial evidence … Quite clearly, this disclosure means that when a carrier foil 1 is removed, the removal can be carried out by a method such as etching in a suitable etchant, or by some other suitable method". The Examiner respectfully disagrees. The Examiner interprets "the carrier foil 1 **can be** removed such as by etching in a suitable etchant …" is not required or optional because Clothier does not provide other method but etching in a suitable etchant. Further, with respect to the appellants' argument of

the "extra/later steps" of Clothier et al, the reply/argument is deemed addressed in the sections above related to the reply/argument to the argument above.

Appellant argues "the Examiner has failed to considered that Asai requires the process to begin with a copper foil 1 on the outer surface of the insulating Resin layer 2 … In contrast, the present invention starts with a printed circuit board and simply applied a dielectric – without further outer copper layer – on this printed circuit board … Thus, because very different structures are involved, the disclosures of Asai and Clothier and not combinable as assert by the Examiner, and any resulting combination would be quite different than Appellant's claimed invention". The Examiner respectfully disagrees. As discussed in the Final Office action, Asai reference is used to teach the missing limitations, such as providing a printed circuit board having circuit traces on at least one side thereof; structuring the dielectric layer for producing vias; and the vias extending through the dielectric layer to the circuit traces. In Col. 2, Lines 58-65, "first, a multi-layer board (a) is prepared by laminating an inner core comprising an inner wiring pattern 3" and this is equivalent to a printed circuit board having circuit traces on at least one side thereof. Clothier et al. and Asai et al. are related to manufacturing a printed circuit board therefore, one ordinary skill in the art would combine these references.

Appellant argues "Thus, neither Clothier nor Asai teaches forming trenches that do not reach circuit traces. In Clothier, there are no circuit traces, as admitted by the Office Action. In Asai, there are no trenches that do not reach the circuit traces. Combination of Clothier and Asai does not provide the missing

elements, at least not without the aid of impermissible hindsight. There is nothing in the description of the formation of circuit traces in Clothier that would suggest modification of Asai's circuit boards to form trenches as well as the vias described by Asai". The Examiner respectfully disagrees. One of ordinary skill in the art would make a substitution of the carrier foil from Clothier to the printed circuit board as taught by Asai. When making a trench for a new trace on the existing printed circuit board, one should not make it through a existing circuit trace because it will be shorted the two traces, as taught by Clothier (Fig. 2c, trenches 4 do not go through the dielectric 3).

Appellant argues "Substitution of the carrier foil by a printed circuit board would be strange to a person skilled in the art and would therefore be non-obvious because such substitution would make no sense ... Therefore, substitution of a printed circuit board the carrier foil 1 in the process of Clothier would not have been obvious". The Examiner respectfully disagrees. One of ordinary skill in the art would substitute the carrier foil for the printed circuit board and apply the method of Clothier for the purpose of adding more traces to the printed circuit board having traces on at least one side thereby reducing cost of manufacturing when making modification to the design.

Appellant argues "Appellant respectfully submits that the Office Actions have proven to much. Since Clothier clearly intends only to form vias that extend all the way though, it makes no sense to selectively stop the process of Clothier at an incomplete, initial point, and then somehow combine this with the teachings of Asai". The Examiner respectfully disagrees. With respect to this argument,

the reply/argument is deemed address in the sections above related to the reply/argument to the rejection above.

C. Rejection of claim 2-11, 15 and 18-22 as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636) and further view of Tamm et al. (US 5666722) should be reversed.

Appellant argues "Claim 2 specifies that the trenches and vias are produced in one single process operation in step c). This is clearly incompatible with the combination of Clothier and Asai for the same reasons as set forth above, and Tamm fails to remedy the short comings of the primary and secondary references". The Examiner respectfully disagrees. With respect to Appellant's reply/argument of the rejection of claim 2; Claims 1, 10, 12-14, 21 and 24 in light of arguments previous set forth in section above, the reply/argument is deemed address in the sections above related to the reply/argument to the rejection above. Furthermore, Tamm et al. is used to teach the missing limitation such as the trenches (24, 25 and 26 Fig. 2b) and vias (23a, Fig. 2c) are produced in one single process operation. Clothier et al., Asai et al. and Tamm et al. are related to manufacturing a printed circuit board therefore, one ordinary skill in the art would combine these references.

Appellant argues "Claims 3-8, 18, 20 and 22 relate to use of a direct-write technique of producing trenches and vias in step c). This is clearly incompatible with the combination of Clothier and Asai for the same reasons as set forth above, and Tamm fails to remedy the shortcomings of the primary and secondary references". The Examiner respectfully disagrees. With respect to Appellant's

reply/argument of the rejection of claims 3-8, 18 20 and 22; Claims 1, 10, 12-14, 21 and 24 in light of arguments previous set forth in section above, the reply/argument is deemed address in the sections above related to the reply/argument to the rejection above.

Appellant argues "Claim 9 specified that the trenched and vias are connected to each other in a landless design … and is not compatible with the asserted combination of Clothier and Asai, and Tamm fails to remedy the shortcomings of the primary and secondary references. The Examiner respectfully disagrees. With respect to Appellant's reply/argument of the rejection of claim 9; Claims 1, 10, 12-14, 21 and 24 in light of arguments previous set forth in section above, the reply/argument is deemed address in the sections above related to the reply/argument to the rejection above.

Appellant argues "Claims 10, 11 and 19 relate to another dielectric layer being deposited and step c) through f) being repeated, and a terminating layer can be applied (claims 11 and 19). These features provide for a buildup of additional layers of circuitry and/or protection of the outer layer, and is not compatible with the asserted combination of Clothier and Asai, and Tamm fails to remedy the shortcomings of the primary and secondary references". The Examiner respectfully disagrees. With respect to Appellant's reply/argument of the rejection of claims 10, 11 and 19; Claims 1, 10, 12-14, 21 and 24 in light of arguments previous set forth in section above, the reply/argument is deemed address in the sections above related to the reply/argument to the rejection above.

Appellant argues "Claim 15 specifies that in step c), when producing trenches, the trenches also comprise vias ... The Office Action refers to Fig. 2b and 2c of Tamm in support of the rejection. However, Tamm discloses sequential formation of a structure that arguably contains a combined trench and vias, in the description of these figures, from col. 4, line 66 to col. 5, line 4. Furthermore, the method of Tamm is not compatible with Clothier or Asai. Accordingly, Appellant submits that claim 15 would not have been obvious over the asserted combination of Clothier, Asai and Tamm". The Examiner respectfully disagrees. With respect to Appellant's reply/argument of the rejection of claim 15; Claims 1, 10, 12-14, 21 and 24 in light of arguments previous set forth in section above, the reply/argument is deemed address in the sections above related to the reply/argument to the rejection above. Furthermore, Tamm et al. is used to teach the missing limitation, when producing trenches and vias in the dielectric in method step c) comprises producing trenches, said trenches also comprising vias (Fig. 2b and 2c).

Appellant argues "Claim 21 specifies that the printed circuit board is a multilayer board comprising two sides and a conductor pattern on both side. This is clearly incompatible with the combination of Clothier and Asai for the same reason as set forth above, and Tamm fails to remedy the shortcomings of the primary and secondary references". With respect to Appellant's reply/argument of the rejection of claim 21; Claims 1, 10, 12-14, 21 and 24 in light of arguments previous set forth in section above, the reply/argument is deemed address in the sections above related to the reply/argument to the rejection above.

Furthermore, Tamm et al. is used to teach the missing limitation, printed circuit board wherein a method of manufacturing printed circuit board where the printed circuit board is a multilayer circuit board comprising two sides and a conductor pattern on each side (Fig. 2f) (Col. 4, Lines 32-35).

D. Rejection of claim 16 as unpatentable as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636) and further view of Konrad et al. (US 2002/0129972) should be reversed.

Appellant argues "Claim 16 specifies that the functional layers are deposited onto the metal layer for electrically contacting electric components. If the asserted combination of Clothier and Asai is made, it does not appear possible to connect the electric components as claimed, and Konrad fails to remedy the shortcomings of the primary and secondary references. Therefore, claim 16 would not have been obvious over the asserted combination for this additional reason". The Examiner respectfully disagrees. With respect to Appellant's reply/argument of the rejection of claim 16; Claims 1, 10, 12-14, 21 and 24 in light of arguments previous set forth in section above, the reply/argument is deemed address in the sections above related to the reply/argument to the rejection above. Furthermore, Konrad reference is used to teach the missing limitation, the functional layers are deposited onto the metal layer for electrically contacting electric component (Par. 49). Clothier et al., Asai et al. and Konrad et al. are related to manufacturing a printed circuit board therefore, one ordinary skill in the art would combine these references.

E. Rejection of claim 17 as unpatentable as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636) and further view of Yokogawa et al. (US 6740416) should be reversed.

Appellant argues "Claim 17 recites that the circuit carrier is manufacturing in a horizontal line. If asserted combination of Clothier and Asai is made, it does not appear possible to connect the electric components as claimed, and Yokogawa fails to remedy the shortcomings of the primary and secondary references. Therefore, claim 17 would not have been obvious over the asserted combination for this additional reason. The Examiner respectfully disagrees. With respect to Appellant's reply/argument of the rejection of claim 17; Claims 1, 10, 12-14, 21 and 24 in light of arguments previous set forth in section above, the reply/argument is deemed address in the sections above related to the reply/argument to the rejection above. Furthermore, Yokogawa reference is used to teach the missing limitation, the circuit carrier is manufacturing in a horizontal line (Col. 18, Lines 53 to Col. 19, Line 8). Clothier et al., Asai et al. and Yokogawa et al. are related to manufacturing a printed circuit board therefore, one ordinary skill in the art would combine these references.

F. Rejection of claim 23 as unpatentable as unpatentable over Clothier et al. (US 2002/0177006) in view of Asai et al. (US 6240636) and further view of Frank et al. (US 5577309) should be reversed.

Appellant argues "Claim 23 specifies that the trenches and vias have a V-shape cross section. This facilitates the electrolytic deposition of metal in the trenches and vias since the depth of the notches is small with respect to the

width of their opening. Frank fails to remedy the shortcomings of the primary and secondary references, so additional of this reference would not have rendered obvious claim23, despite that the shape of the vias may be similar. The Examiner respectfully disagrees. With respect to Appellant's reply/argument of the rejection of claim 23; Claims 1, 10, 12-14, 21 and 24 in light of arguments previous set forth in section above, the reply/argument is deemed address in the sections above related to the reply/argument to the rejection above. Furthermore, Frank reference is used to teach the missing limitation, the trenches have a V-shape cross section. Clothier et al., Asai et al. and Frank et al. are related to manufacturing a printed circuit board therefore, one ordinary skill in the art would combine these references.

In conclusion, the claims on appeal are not novel as it pertains to a method of manufacturing a circuit carrier and the use of the method. The examiner has provided proper evidence support prima facie case of obviousness with respect to the rejection assert above. The examiner respectfully requests that the rejection of the claims be affirmed and that such claims be indicated are not inventive or allowable over the prior art.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/HUNG D NGUYEN/

Examiner, Art Unit 3742

Conferees:

/Henry Yuen/

Supervisory Patent Examiner, TC 3700

/TU B HOANG/

Supervisory Patent Examiner, Art Unit 3742